1. A method of forming a highly dislocation free compound semiconductor on a lattice mismatched substrate 24, comprising:

depositing a polycrystalline buffer layer 22 on the substrate;

creating an amorphous layer 28 at an interface of the substrate and the polycrystalline buffer layer; and

depositing a monocrystalline template layer 30 of the compound semiconductor on the buffer layer.

2. The method of claim 1, further comprising:

growing an epilayer 32 of the compound semiconductor on the template layer 30.

3. The method of claim 1, wherein said amorphous layer 28 is created by ion implantation.

4. The method of claim 3, wherein said amorphous layer 28 is created by ion implantation through the polycrystalline buffer layer 22.

5. The method of claim 3, wherein said amorphous layer 28 is created by back-side ion implantation through the substrate 24.

6. The method of claim 1, wherein said amorphous layer 28 comprises an amorphous oxide layer.

7. The method of claim 1, wherein said compound semiconductor comprises a III-V material.

8. The method of claim 7, wherein said III-V material comprises $Al_x In_y Ga_{1-x-y}N$ ($0 < x, y < 1$).

9. The method of claim 8, wherein said amorphous layer 28 comprises an amorphous oxide layer created by oxygen ion implantation.

10. The method of claim 9, wherein said polycrystalline buffer layer 22 and said template layer 30 exhibit homoepitaxy.

11. The method of claim 10, wherein said polycrystalline buffer layer 22 and said monocrystalline template layer 30 comprise a same material.

12. The method of claim 1, wherein said monocrystalline template layer 30 is closely lattice matched to the polycrystalline buffer layer 22.

13. The method of claim 12, wherein said buffer layer 22 serves as a seed layer for growth of said template layer 30, and further comprising:

growing a compound semiconductor based device structure on the template layer 30.

14. The method of claim 13, wherein said compound semiconductor comprises $Al_x In_y Ga_{1-x-y} N$ $(0 < x, y < 1)$.

15. The method of claim 14, wherein said amorphous layer 28 is created by ion implantation after the buffer layer 22 is deposited on the substrate 24, and the substrate comprises a material that becomes amorphous by ion implantation.

16. The method of claim 15, wherein said substrate 24 comprises one of: Si, SOI, and $Al_x Ga_{1-x} As$ (where $x>0$).

17. The method of claim 15 wherein said polycrystalline buffer layer 22comprises AlN.

18. The method of claim 15, wherein said amorphous layer 28 is created by nitrogen ion implantation.

19. A semiconductor structure comprising:
a semiconductor substrate 24;
a polycrystalline buffer layer 22 on the substrate;
an amorphous layer 28 at an interface of the substrate and the buffer layer; and
an epilayer 32 of monocrystalline compound semiconductor on the buffer layer.

20. The structure of claim 19, wherein said epilayer 32 includes a monocrystalline template layer 30 of said compound semiconductor grown on said buffer layer 22.

21. The structure of claim 19, wherein said epilayer 32 comprises a compound semiconductor based device structure.

22. The structure of claim 21, wherein said amorphous layer 28 comprises an amorphous oxide layer, and said buffer layer 22 and epilayer 32 are closely lattice matched.

23. The structure of claim 19, wherein said compound semiconductor comprises $Al_x In_y Ga_{1-x-y} N$ ($0 < x, y < 1$).

24. The structure of claim 23, wherein said epilayer 32 has a dislocation density below $10^5$ $cm^{-2}$

25. The structure of claim 23, wherein said polycrystalline buffer layer 22 comprises AlN.

26. A semiconductor structure comprising:

a semiconductor substrate 24;

a polycrystalline buffer layer 22 on the substrate;

an amorphous layer 28 at an interface of the substrate and the buffer layer; and

a monocrystalline template layer 30 of compound semiconductor on said buffer layer.

27. The structure of claim 26, wherein said amorphous layer 28 comprises an amorphous oxide layer, and said buffer layer 22 and template layer 30 are closely lattice matched.

28. The structure of claim 26, wherein said compound semiconductor comprises: $Al_x In_y Ga_{1-x-y} N$ ($0 < x, y < 1$).

29. The semiconductor structure of claim 26, wherein said polycrystalline buffer layer 22 comprises AlN.